



American National Standard  
ANSI E1.11 – 2008 (R2018)  
Entertainment Technology—USITT DMX512-A  
Asynchronous Serial Digital Data  
Transmission Standard for Controlling  
Lighting Equipment and Accessories

Document number: CP/2007-1013r3.1

This document was approved as an American National Standard by the ANSI Board of Standards Review on 31 May 2018. It is a reaffirmation of the 2008 edition of the Standard.

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The ESTA Technical Standards Program was created to serve the ESTA membership and the entertainment industry in technical standards related matters. The goal of the Program is to take a leading role regarding technology within the entertainment industry by creating recommended practices and standards, monitoring standards issues around the world on behalf of our members, and improving communications and safety within the industry. ESTA works closely with the technical standards efforts of other organizations within our industry, including USITT, and VPLT, as well as representing the interests of ESTA members to ANSI, UL, and the NFPA. The Technical Standards Program is accredited by the American National Standards Institute.

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The Control Protocols Working Group, which authored this Standard, consists of a cross section of entertainment industry professionals representing a diversity of interests. ESTA is committed to developing consensus-based standards and recommended practices in an open setting.

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**Foreword**

*(This foreword contains no requirements and is not part of E1.11.)*

This Standard describes a method of digital data transmission between controllers and controlled lighting equipment and accessories, including dimmers and related equipment. This Standard is intended to provide for interoperability at both communication and mechanical levels with controllers made by different manufacturers.

There are five normative annexes in this Standard. These address extensions of the base standard and are considered part of the Standard, which means that when an extension described in an Annex is implemented, compliance with the annex is mandatory. However, a product compliant with the Standard can be manufactured without implementing these annexes.

The original version of the DMX512 Standard was developed in 1986 by the Engineering Commission of the United States Institute for Theatre Technology, Inc. (USITT). Minor revisions were made in 1990. DMX512 has gained international acceptance throughout the entertainment industry, even though USITT is not formally accredited as a standards making body. The earlier versions of this Standard covered only data used by dimmers. In practice this Standard has been used by a wide variety of devices; this version recognizes that fact.

In 1998, it became evident that additional updates to the Standard were necessary and formal recognition through an internationally recognized standards organization was required. USITT issued a Call for Comments in order to solicit recommendations for changes to the Standard. At the same time, USITT transferred maintenance of DMX512 to ESTA's ANSI-accredited Technical Standards Program, now operating as ESTA's Technical Standards Program.

A Task Group established under the TSP's Control Protocols Working Group acted on the proposals received in response to the Call for Comments. The primary goal was to make editorial updates to DMX512 appropriate for current times, including the addition of technical features while maintaining a balance with backward compatibility. Many proposals, while technically innovative, could not be accepted because their implementation would not have been backward compatible and would have immediately rendered obsolete most of the installed base of equipment.

In 2004, as a result of the actions taken on those proposals and subsequent development under the *Policies and Procedures* of the ESTA Technical Standards Program, E1.11-2004 was approved as an American National Standard. Despite being an American National Standard, development has had strong international participation and support.

Beginning in 2007, based on comments and requests from users and manufacturers, minor revisions were made to E1.11-2004 and submitted to the public for review and comment. These changes included defining one of the reserved Alternate START Codes for UTF-8 text packets, a note emphasizing refresh timings, and removal of the informative PICS (Protocol Implementation Compliance Statement) clauses. The PICS clauses were simply a summary of the mandatory requirements of the standard, but often had to employ language that used double negatives and led to confusion about some requirements. The 2008 edition was the result of those revisions to the 2004 edition. This edition is a reaffirmation of the 2008 edition.

## 1 General

### 1.1 Scope

This Standard describes a method of digital data transmission between controllers and controlled equipment as described in Clause 1.4 and accessories, including dimmers. It covers electrical characteristics, data format, data protocol, and connector types.

This Standard is intended as a guide for:

1. Equipment manufacturers and system specifiers who wish to integrate systems of lighting equipment and accessories, including dimmers, with controllers made by different manufacturers.
2. Equipment manufacturers seeking to implement a standard digital transmission protocol in their lighting control and accessory products.
3. System specifiers and designers to gain detailed information about allowed connectors and allowed system topologies.

This standard is not intended to replace existing protocols other than USITT DMX512 and DMX512/1990. Cable requirements and premises wiring are not within the scope of this Standard.

Equipment compliant with this Standard will be marked DMX512-A or USITT DMX512-A in order to distinguish it from the previous (informally recognized) versions. Unless otherwise noted, references to DMX512 in this document refer to DMX512-A.

### 1.2 Overview and Architecture

This standard uses a simple asynchronous eight-bit serial protocol consisting of an untyped byte stream produced by standard UARTs. The physical media, not addressed in this document, is normally, but not exclusively, a two-pair cable, with each pair serving as a data link. The media is driven using ANSI/TIA/EIA-485-A-1998 (hereafter referred to as EIA-485-A in this document) balanced data transmission techniques. Physical connection at devices is via 5-pin XLR connectors or by "hard-wiring" to terminals. Restricted use of connectors other than 5-pin XLR is allowed if certain conditions apply (see clause 7).

Data on the primary data link is sent in packets of up to 513 slots. The first slot is a START Code, which defines the information in the subsequent slots in the packet. The interoperability of equipment complying with the Standard is largely due to the use of the NULL START Code by transmitting devices. Proper function is dependent upon the receiving device(s) extracting the pertinent data for processing from each transmitted packet.

Data on the secondary data link, when implemented, is used for a variety of purposes, all of which fall within the scope of EIA-485-A. Identification of the required circuit topology for any particular implementation is defined.

### 1.3 Appropriate uses of this Standard

Equipment designers and general users of this Standard will recognize that this Standard is intended to fill only a limited range of uses. Other standards will be more appropriate for different uses. This is not intended to support a venue wide network that can carry data for lighting, sound, and scenery mechanization, for example, all on the same wire.

This Standard does not require mandatory error checking of NULL START Code packets. There is no assurance that all DMX512 packets will be delivered. It is common practice for merge units and protocol converters to drop packets that they cannot process in a timely manner. The 1986 and 1990 versions of the USITT Standard specifically allow dimmers to ignore packets that they cannot process in a timely manner, and this concept survives in this version of the Standard with respect to NULL START Code packets.

**1.4 Classes of data appropriate for transmission over links designed to this Standard**

DMX512 is designed to carry repetitive control data from a single controller to one or more receivers. This protocol is intended to be used to control dimmers, other lighting devices and related non-hazardous effects equipment.

**1.5 Classes of data not appropriate for transmission over links designed to this Standard**

Since this Standard does not mandate error checking, DMX512 is not an appropriate control protocol for hazardous applications.

**1.6 Compliance**

Compliance with this Standard is strictly voluntary and the responsibility of the manufacturer. Markings and identification or other claims of compliance do not constitute certification or approval by the E1 Accredited Standards Committee. See clause 10 for Marking and Disclosure requirements.

**2 Normative references**

ANSI/TIA/EIA-568-B-2001	Commercial Building Telecommunications Cabling Standard
ANSI/TIA/EIA-485-A-1998	Electrical Characteristics of Generators & Receivers for Use in Balanced Digital Multipoint Systems

This standard will be referred to as EIA-485-A in this document.

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Note: EIA-485-A is compatible with: ISO/IEC 8482:1993 Information Technology - Telecommunications and information exchange between systems - Twisted pair multipoint interconnections.

ISO/IEC 646 Information Technology - ISO 7-bit Coded Character Set for Information Interchange

IEC 60603-7 Connectors for Frequencies Below 3 MHz for Use with Printed Wiring Boards - Part 7: Detail Specification for Connectors, 8-Way, Including Fixed and Free Connectors with Common Mating Features, with Assessed Quality

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USITT DMX512/1990 Digital Data Transmission Standard for Dimmers and Controllers

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### 3 Definitions

**3.1 Asynchronous:** signals that start at any time and are not locked or synchronized to the receiving device by a separate clock line.

**3.2 Balanced Transmission Line:** a data communications line where two wires are present, the signal and its opposite (complement), the actual signal being the difference between the voltages on the two wires. Balanced lines have excellent noise and interference rejection properties.

**3.3 Break:** a high (mark) to low (space) transition followed by a low of at least 88 microseconds followed by a low to high transition.

**3.4 Circuit Common:** the common reference (zero volt supply) of the EIA-485-A driver or receiver circuitry.

**3.5 Common:** see Data Link, Signal Common, and Circuit Common.

**3.6 Common Mode Voltage:** a voltage appearing equally on the data+ (plus) and data- (minus) lines relative to circuit Common.  $V_{cm} = (V_a + V_b)/2$  where:

$V_{cm}$  is the Common Mode Voltage

$V_a$  is the voltage on DMX512 data+ with respect to circuit Common

$V_b$  is the voltage on DMX512 data- with respect to circuit Common

**3.7 Controller:** a transmitting device that originates DMX512 data.

**3.8 Data+:** signal true.

**3.9 Data-:** signal complement.

**3.10 Data Link:** physical connection between transmitting and receiving devices.

**3.11 Data Link Common:** the connection to circuit Common at the point of interconnection (DMX512 Port) of the product.

**3.12 DMX512 Port:** a DMX512 signal connection point (connector or terminal strip).

**3.13 DMX512 Processing Device:** a piece of equipment that regenerates the timing of any DMX512 packet or has provision for other signal inputs from which the outgoing DMX512 packet is generated. In the absence of any DMX512 transmitting capability, the device has provision for other signal outputs that are controlled in some manner by the incoming DMX512 packet. Basic buffer products are not normally considered processing devices.

**3.14 Earth Ground:** the common, zero potential available from the mains electricity supply and usually connected to the metal chassis of equipment. Earth Ground is referred to as Earth in Europe and Ground in the USA.

**3.15 Enhanced Functionality:** use of the optional secondary data link of a DMX512 port and/or optional additional use of the primary data link of a DMX512 port.

**3.16 Idle:** the time between slots that the DMX512 line is high and not sending any information (also known as the 'Mark' condition).

**3.17 In-Line Device:** any component that receives and re-transmits DMX512.

**3.18 Isolated:** circuit topology in which the output is completely electrically disconnected from the input.

**3.19 Legacy (as used in this Standard):** transmitting and receiving devices complying with the original USITT DMX512 or DMX512/1990 in all aspects of those standards. (Exception: receiving devices that are not dimmers but comply with all other aspects of DMX512/1990 are considered to be Legacy Equipment.)

**3.20 Line Driver:** an electrical circuit providing differential voltage excursions on a data link, operating within a defined Common Mode voltage range and with a specified response to overload and overvoltage conditions. Sometimes simply referred to as a “driver.”

**3.21 Line Receiver:** an electrical circuit allowing detection of differential voltage excursions on a data link, operating within a defined Common Mode voltage range and with a specified response to overload and overvoltage conditions.

**3.22 Loop-Through Connection:** a connector or terminal DMX512 port that connects the signals Data 1+, Data 1- and Data link common, and optionally Data 2+ and Data 2-, of one DMX512 port to another DMX512 port. Frequently abbreviated to Loop or Thru.

**3.23 Manufacturer ID:** a two-byte value assigned to a Manufacturer/Organization by the E1 Accredited Standards Committee for use with specific Alternate START Codes. This ID identifies the data contained in the packet as proprietary. This packet may be safely ignored by systems that do not implement the specific start code.

**3.24 Mark:** a line condition where Signal True is high with respect to Signal Complement. A Mark represents a binary 1.

**3.25 MAB (MaB):** Mark After Break – the period of time between the low to high transition that signifies the end of Break and the high to low transition which is the start bit of the START Code (slot 0).

**3.26 MBB (MbB):** Mark Before Break – the period of time between the end of the second stop bit of the last slot and the high to low transition that signifies the start of Break.

**3.27 Merge Unit:** a product comprising one or more receiving devices and one or more transmitting devices that generate a DMX512 packet derived from the manufacturers declared logical combination of the DMX512 input packets.

**3.28 NULL START Code:** a START Code with a value of zero (00h).

**3.29 Packet (in DMX512-A):** a Reset Sequence followed by all slots up to the Mark Before Break.

**3.30 Receiver (Receiving Device):** a piece of equipment that accepts a DMX512 signal.

**3.31 Refresh Rate:** the number of DMX512 packets with a NULL START Code sent per second.

**3.32 Reset Sequence:** a sequence of a Break, Mark After Break, and START Code.

**3.33 Signal Common:** the common reference conductor of the physical media (e.g., the cable shield).

**3.34 Slot:** a sequentially numbered framed byte in a DMX512 packet. A single Universe contains a maximum of 513 Slots, starting at slot 0. Slot 0 is the START Code. Slots 1 through 512 are data slots.

**3.35 Slot Footprint:** the number of data slots used by a product in its operation.

*Note: A 24 way dimmer rack may have a footprint of 24, it may be more if some slots are used to provide additional control functions using NULL START Code packets. Automated luminaires usually require a Slot Footprint of greater than one.*

**3.36 Space:** a line condition where Signal True is low with respect to Signal Complement. A Space represents a binary 0.

**3.37 Start Bit:** the additional bit attached to the beginning of a byte to indicate to the receiver that a new byte is being sent. The start bit is always low, i.e., Space.

**3.38 START Code:** the first slot sent after Break, indicating the type of information to follow.

**3.39 Stop Bit:** the additional bit(s) attached to a byte to indicate the end of the byte – DMX512 has 2 stop bits. The stop bit is always high, i.e., Mark.

**3.40 Terminator:** a device or circuit topology that is designed to minimize unwanted signal reflections on a data link.

**3.41 Transmitting Device:** a piece of equipment that produces a DMX512 signal.

**3.42 UART:** Universal Asynchronous Receiver/Transmitter. A device that generates and/or decodes serially transmitted data.

**3.43 Universe:** a DMX512 data link originating from a single DMX512 source. Control of up to 512 DMX512 data slots comprises a single universe.

## 4 Electrical Specifications and Physical Layer

### 4.1 General

The electrical specifications of this Standard are those of EIA-485-A, except where specifically stated in this document. Where a conflict between EIA-485-A and this document exists, this document is controlling as far as this Standard is concerned.

The physical layer of a DMX512 data link is constrained by earth grounding practices, termination methods, signal levels, EMC, and accidental damage by connection to other devices.

In addition to complying with the requirements of EIA-485-A, clauses 5 and 6 specify additional requirements not addressed by EIA-485-A.

### 4.2 Electrical isolation

EIA-485-A makes no general provisions for electrical isolation, however, this Standard does. Suitable optical isolation, transformer isolation, or other means may be employed to prevent the undesirable propagation of voltages that exceed the Common Mode limits of EIA-485-A (see clauses 5 and 6). The inclusion of such isolation does not, however, alter the requirement that a transmitter or receiver conforms to EIA-485-A.

### 4.3 Topology

A data link shall consist of a single active differential line driver, a terminated transmission line and one or more differential line receivers meeting the requirements of EIA-485-A and all additional requirements of this Standard. A DMX512 controlled device capable of returning status information is referred to as a responder in this Standard. For the purposes of this Standard, responders are considered to fall under the category of receiving devices. This subject is covered in Annex B.

#### 4.4 DMX512 ports

A DMX512 Port is the signal connection point between the internal electronics of a device and the physical transmission line (cable), referred to as the equipment interconnect points by EIA-485. It may be made either by the prescribed connector as defined in clause 7 or by a terminal strip. A DMX512 port carries four signals and a common reference, designated data 1-, data 1+, data 2-, data 2+, and data link common. (In some situations, data 2- and data 2+ are not connected /provided). Historically, these signals have been referred to as Pins which correlates to the physical pinout used on the XLR style connectors as defined in clause 7 of this Standard. There are other situations where different physical connections may be encountered, such as a terminal strip.

#### 4.5 Data link common and grounding topologies

Various portions of clause 5 and Annex A deal with shield-to-earth ground topologies. In all cases there is a low impedance connection between data link common pin or contact of the DMX512 port and signal common of the EIA-485-A driver or receiver circuitry.

#### 4.6 Preferred method of earth grounding data link common

DMX512 systems should make use of earth ground referenced transmitting devices and isolated receiving devices. This approach provides for a single point solid ground/chassis connection at the source, and allows for variations in building ground potentials between transmitting and receiving devices. This is to ensure that interoperability of equipment is achieved in situations that might otherwise exceed the Common Mode limitations of EIA-485-A. See EIA-485-A clause 4.3.1. Other approaches are covered in Annex A.

#### 4.7 Primary data link

Data 1- and Data 1+ of a DMX512 Port form the primary data link. Format of the data is covered in clause 8. Limited use of multiple data link drivers for half-duplex, bi-directional data transmission on the primary data link is permitted in accordance with Enhanced Functionality as described in Annex B.

#### 4.8 Secondary data link

Implementation of the secondary data link is optional.

##### 4.8.1 Secondary data link - active use

Data 2- and Data 2+ of a DMX512 Port provide a secondary EIA-485-A data link. Implementation of this data link is optional. Several different network topologies are associated with the implementation of the secondary data link. Use of the secondary data link is permitted only in accordance with Enhanced Functionality as described in Annex B.

##### 4.8.2 Secondary data link - passive loop through ports

In order to extend Enhanced Functionality across a network, devices containing two DMX512 ports, one for receive and one for transmit, that do not actively process or buffer data, shall provide a direct passive link for all signals between the two ports. Devices containing three or more DMX512 ports may provide a passive link between only two of the ports. These two ports shall be declared as required in Clause 10 and should be marked on the product. In order to enhance interoperability of DMX512 products, equipment designers are encouraged to provide passive loop through on the secondary data link pins or contacts whenever possible, even if not required per this clause.

#### 4.9 Data link termination procedures

DMX512 data links shall be terminated to eliminate ringing and signal reflection, which can cause mis-operation of an otherwise properly designed system. To comply with this Standard, all equipment connected to a DMX512 data link shall operate in accordance with the stated manufacturer's specification when the data link is terminated. The terminator shall be a 120 ohm +5%/-10% impedance placed between Data+ and Data-. In the preferred topology where the transmitter is connected to one end of the data link, the far end of the data link shall be terminated. In the case where the transmitter cannot be connected at one end of the data link, then both

ends of the data link shall be terminated. Manufacturers of receiving devices may provide internal termination of the data link. Where such termination is provided, it shall comply with the electrical and marking requirements of this Standard. It is recommended that termination components be chosen to withstand continuous voltages of at least 30 VAC 50 Hz/42 VDC.

#### 4.10 Unpowered devices

Unpowered connected DMX512 devices shall not degrade the performance of the DMX512 transmission system nor materially lower the impedance they present to the data link.

### 5 Nominal Operating Characteristics

#### 5.1 General

Operation limits generally follow the detailed requirements of EIA-485-A. Where appropriate, separate limits are given for isolated products. All electrical characteristics shall be measured at the DMX512 ports of the product.

#### 5.2 Chassis in power isolated equipment

In equipment where connection to protective grounding is not made concurrent with power connection, such as battery powered equipment or equipment powered by isolated low voltage transformers, chassis is deemed to include any exposed metal DMX512 connector parts which do not carry signals.

#### 5.3 Earth grounding of data link common for transmitters

In recognition of the need for DMX512 compliant products to be capable of interconnection as part of large and potentially complex systems, this Standard defines two allowable topologies for the earth grounding of data link common and circuit common for transmitters, to be known as "Ground Referenced" and "Isolated". The preferred method is "Ground Referenced." "Isolated" is covered in Annex A.

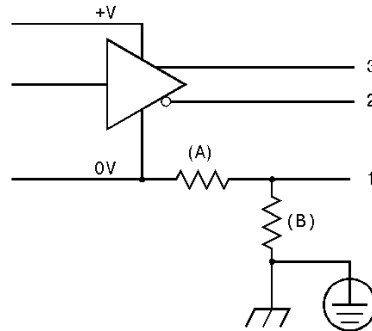
#### 5.4 Ground referenced transmitters

Ground referenced transmitting device outputs shall meet the following conditions in table 1 during normal operation under open circuit condition.

**Table 1 - Ground Referenced Transmitter Characteristics**

Connection	Limit (measured at port pin or contact)	Comment
Data 1+ to Data Link Common or Data 1- to Data Link Common	$0 < v < +6$ VDC	
Data 2+ to Data Link Common or Data 2- to Data Link Common	$0 < v < +6$ VDC	Enhanced Function devices only
Data Link Common to Chassis	0V	
Data 1- to Chassis or Data 1+ to Chassis	$0 < v < +6$ VDC	
Data 2- to Chassis or Data 2+ to Chassis	$0 < v < +6$ VDC	Enhanced Function devices only
Data 1- to Data1+	+/- 6V (open circuit)	
Data 2- to Data 2+	+/- 6V (open circuit)	

Figure 1 illustrates a ground referenced transmitter port. It is characterized by the direct connection of the shield (Data Link Common) to chassis and protective earth. Therefore, devices employing ground referenced transmitters shall be provided with provision for connection to protective earth. Any resistance (A) between Data Link Common's pin or contact and zero volt supply (circuit common) of the transmitter circuit shall be less than 100 ohms. Any resistance (B) between Data Link Common's pin or contact and chassis shall be less than 20 ohms and is preferably zero ohms.



## Figure Key

- 1 - DMX512 Data Link Common
- 2 - DMX512 Data 1- (or Data 2-)
- 3 - DMX512 Data 1+ (or Data 2+)
- A - Optional Resistance (see text)
- B - Optional Resistance (see text)

Figure 1 - Ground Referenced Transmitter

A DMX512 device may have any number of Ground Referenced transmitter ports. Ground Referenced transmitter ports may be used by all DMX512 devices including ones that provide any number of non-DMX512 input or output ports. Adherence to this topology allows a DMX512 transmitter connector to be marked as shown in table 9.

Because the transmitter in this topology is grounded, the existence of an isolation barrier between the transmitter and any other part of the device shall NOT qualify output for marking as ISOLATED.

### 5.5 Disallowed transmitter topology

The Figure 2 configuration is not permitted, although it may exist on some legacy products. While this topology is described as one possible topology in EIA-485-A, it is not appropriate when considering operation of DMX512 transmitting devices in systems encountering differential ground potentials.

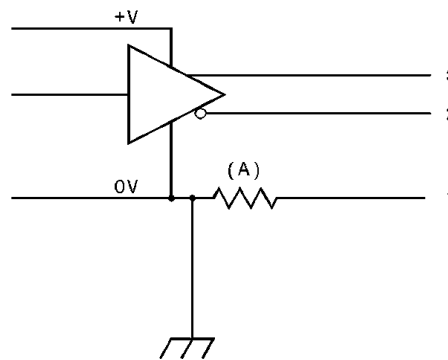


Figure Key

- 1 - DMX512 Data Link Common
- 2 - DMX512 Data 1- (or Data 2-)
- 3 - DMX512 Data 1+ (or Data 2+)
- A -  $R > 0.2 \text{ ohm}$

Figure 2 - Transmitter Topology NOT Allowed

### 5.6 Earth grounding of data link common for receivers

This Standard defines several allowable topologies for earth grounding of data link common and circuit common for receiving devices. These are to be known as “non-isolated” and “isolated”. The preferred method is “isolated.” A specific concession is available to manufacturers of non-isolated receivers who, for reasons beyond the scope of this Standard, require a direct link between data link common and chassis. Non-isolated and grounded receivers are addressed in Annex A.

### 5.7 Isolated receiver characteristics

For isolated devices, a capacitor may be fitted between Data Link Common and chassis for the purpose of Radio Frequency bypass. Devices shall continue to operate correctly when exposed to any of the conditions in table 2.

**Table 2 - Isolated Receiver characteristics**

Connection	Limit (measured at port pin or contact)	Comment
Data 1- to Data Link Common or Data 1+ to Data Link Common	+12 / -7 VDC	Common Mode range
Data 2- to Data Link Common or Data 2+ to Data Link Common	+12 / -7 VDC	Enhanced Functionality devices only
Data Link Common to Chassis	> 22M ohm @ 42 VDC	
Data 1- to Chassis or Data 1+ to Chassis	> 22M ohm @ 42 VDC	
Data 2- to Chassis or Data 2+ to Chassis	> 22M ohm @ 42 VDC	Enhanced Functionality devices only
Data 1- to Data 1+	+/- 6 V	
Data 2- to Data 2+	+/- 6 V	Enhanced Functionality devices only
Any Port Pin or Contact to Chassis	30 VAC / 42 VDC	

Figure 3 illustrates an isolated receiver. Any signal pin or contact of the DMX512 isolated receiver shall present a resistance (B) greater than 22 Mohm at 42 VDC with respect to Chassis, with respect to Protective Ground (where fitted), with respect to any other signal inputs or outputs, and with respect to other ground referenced electronics. There may be a capacitance (not shown) between Data Link Common and chassis for Radio Frequency bypass. Any resistance (A) between Data Link Common's pin or contact and zero volt supply (circuit common) supply of the receiver circuit shall be less than 100 ohms.

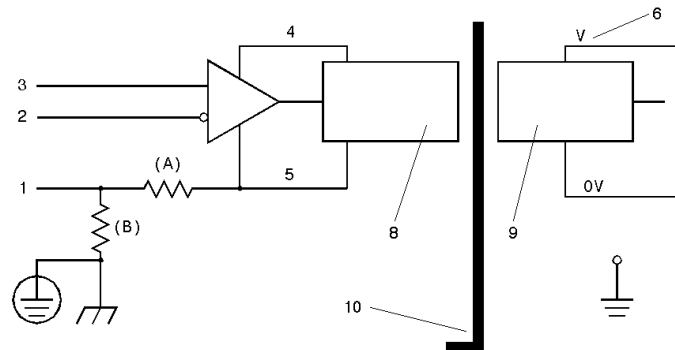


Figure Key

- |                                 |                                       |
|---------------------------------|---------------------------------------|
| 1 - DMX512 Data Link Common     | 9 - Optional Non-Isolated Electronics |
| 2 - DMX512 Data 1- (or Data 2-) | 10 - Isolation Barrier                |
| 3 - DMX512 Data 1+ (or Data 2+) | A - Optional resistance (see text)    |
| 4 - Isolated Supply             | B - Optional resistance (see text)    |
| 5 - Isolated 0V Supply          |                                       |
| 6 - V (+ or -)                  |                                       |
| 7 - I / O                       |                                       |
| 8 - Isolated Electronics        |                                       |

Figure 3 - Isolated Receiver

Adherence to this topology allows a DMX512 receiver port to be marked as ISOLATED. Isolated receiver ports may be used by all DMX512 devices including ones that provide any number of non-DMX512 input or output ports. A DMX512 device may have any number of isolated receiver ports

### 5.8 Disallowed receiver topology

Figure 4 configuration is not permitted, although it may exist on some legacy products. While this topology is described as one possible topology in EIA-485-A, it is not appropriate when considering operation of DMX512 receiving devices in systems encountering differential ground potentials.



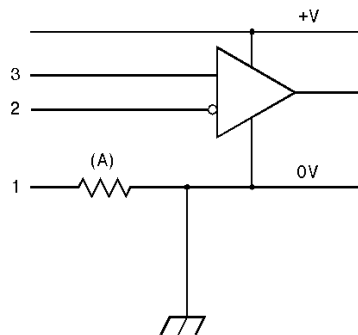


Figure Key

- 1 - DMX512 Data Link Common
- 2 - DMX512 Data 1- (or Data 2-)
- 3 - DMX512 Data 1+ (or Data 2+)
- A -  $R \geq 0.2$  ohm

Figure 4 - Receiver Topology NOT Allowed

### 5.9 DMX512 processing devices

It is permissible to design processing devices based on the Isolated Receiver / Ground Referenced Transmitter or Isolated Receiver / Isolated Transmitter models (see Annex A) already described.

### 5.10 Loading designation

As per EIA-485-A, the total load permitted on a DMX512 data link is 32 unit loads. Transmitters designed for this Standard shall be capable of driving 32 unit loads on a DMX512 data link. Each receiving port on a DMX512 device shall have a unit load of 1 or less as per EIA-485.A receiver biased to any voltage from -7 to +12 volts shall not present a capacitive load to the line of more than 125 pF per unit load.

Declaring or marking of the unit load is not required by this Standard. If a manufacturer chooses to declare or mark their products with a unit load value, the declared or marked value shall be the greater of either the DC unit load determined by EIA-485-A clause 4.1 or the unit load as determined by the capacitive loading. In either case, if the unit load is declared the capacitive load values shall also be declared.

## 6 Protection

### 6.1 Minimum protection against interconnection damage

Clause 4.2 of EIA-485-A recognizes that certain other extraneous conditions may overstress the system and that these conditions should be specified in the referencing standard. Extensive use of temporary and portable equipment in Entertainment Lighting Industry results in frequent connection and disconnection of equipment and gives rise to the possibility of equipment misconnection.

Equipment may be protected against damage resulting from accidental connection to voltages in excess of the minimum defined in EIA-485-A clauses 4.2.5 and 4.2.6, and this is recommended. See Annex C for

requirements allowing DMX512 ports to be declared “DMX512-A Protected”. This does not negate the need to comply with EIA-485-A clause 4.2.6 - Transient overvoltage tolerance.

## 6.2 Minimum Electro Static Discharge (ESD) protection

Manufacturers shall ensure that any port pin or contact can withstand a minimum of 4kV ESD for contact discharge and 8kV ESD for air discharge in accordance with IEC 61000-4-2 or other local regulations that may require higher levels of protection. The acceptance criteria for this requirement allows for temporary loss of function, provided the function is self recoverable or can be restored by the operation of controls. Meeting this requirement does not alter the fact that a manufacturer may have to meet other more stringent ESD requirements to conform to local EMC regulations.

## 7 Connection Methods

### 7.1 Equipment fitted with user accessible pluggable data link connections

This category includes all portable products.

Female connectors shall be used on controllers and other transmitting devices (primary data link) and male connectors shall be used on receiving devices. Female and male connectors consistent with this convention shall also be used where loop-through connections are provided.

#### 7.1.1 Required connector

Equipment in this category shall use 5-pin XLR connectors with the physical pinout of the 5-pin XLR in accordance with Table 3.

**Table 3- Signal designations summary**

Use	5-Pin XLR Pin #	DMX512 Function
Common Reference	1	Data Link Common
Primary Data Link	2	Data 1-
	3	Data 1+
Secondary Data Link (Optional - see clause 4.8)	4	Data 2-
	5	Data 2+

#### 7.1.2 Concession for use of an alternate connector (NCC DMX512-A)

A concession to use an alternate connector is available only when it is physically impossible to mount a 5-pin XLR connector on the product. In such cases all the following additional requirements shall be met :

- 1) The alternate connector shall not be any type of XLR connector.
- 2) The alternate connector shall not be any type of IEC 60603-7 8-position modular connector except as allowed in clause 7.3.
- 3) Provided that all other requirements of this Standard are met, in addition to the declaration in the equipment manual, the alternate connector shall be marked as NCC DMX512-A (Not Connector Compatible). If such a marking is not physically possible at the connector, an appropriate marking shall be made elsewhere on the equipment. The pin numbering on the alternate connector should match numbering for the standard 5-Pin XLR connector.
- 4) The manufacturer shall make available an adapter with the appropriate connections to a standard 5-pin XLR connector for all DMX512 ports included in the alternate connector.
- 5) The Enhanced Functionality, if applicable, and ground/isolation declarations shall continue to be declared for each DMX512 port.

### 7.2 Equipment intended for fixed installation with internal connections to the data link

Fixed installation products with internal connections to the data link may use the 5-pin XLR connector, but shall

not use any other XLR connector. When use is made of the 5-pin XLR connector, the requirements of 7.1 and 7.1.1 shall apply. When a non-XLR connector is used, this Standard makes no other restriction or stipulation on connector choice. The contact (pin) numbering on the alternate connector should match numbering for the standard 5-Pin XLR

### 7.3 IEC 60603-7 8-position modular connectors

The use of IEC 60603-7 8-position modular connectors (commonly referred to as RJ45 type connectors – plugs/jacks) and associated punchdown terminal blocks shall be limited to connections that are part of a fixed installation and not normally accessible except to qualified, authorized users, nor intended for regular connection and disconnection. External (user accessible) IEC 60603-7 8-position modular connectors are permitted only on patch and data distribution products and only when permanently installed in controlled access areas.

*Note: Examples of not normally accessible or controlled access areas include a locked electrical room or control booth, provided those who need access have a key (or lock combination) available.*

**Table 4 - Connection Schedule for DMX512 Equipment Using IEC 60603-7 8-Position Modular Connectors**

Pin (Wire) #	Wire Color	DMX512 Function
1	white / orange	data 1+
2	orange	data 1-
3	white / green	data 2+ (optional)
6	green	data 2- (optional)
4	blue	Not assigned
5	white / blue	Not assigned
7	white / brown	Data Link Common (Common Reference) for Data 1 (0 v)
8	brown	Data Link Common (Common Reference) for Data 2 (0 v)
	drain	

*Note 1: Pin numbering and color in accordance with ANSI/TIA/EIA-568 scheme T568B.*

*Note 2: Pin 8 should be wired as signal common even if pins 3 and 6 are NOT wired so that both conductors 7 and 8 are at equal potential.*

**Warning:** Accidental connection to non-DMX512 equipment likely to be encountered (e.g., an Ethernet Hub at a patch bay) may result in damage to equipment. Pins 4 and 5 may carry voltages outside the EIA-485 range in telecom applications (e.g., telephone ringing). Pins 4 and 7 may carry voltages outside the EIA-485 range in other applications (e.g., some manufacturers whose distributed DMX512 buffering products require low voltage DC power may use these wires for this purpose). Because of these various uses, misplugging unlike systems could cause serious damage.

## 8 Data protocol

### 8.1 Format

DMX512 slots shall be transmitted sequentially in asynchronous serial format, beginning with slot 0 and ending with the last implemented slot, up to slot 512 (a maximum total of 513 slots). Prior to the first data slot being transmitted, a Reset Sequence shall be transmitted – a BREAK, followed by a MARK AFTER BREAK, and a START Code. Valid DMX512 data slot values under a NULL START Code shall be 0 to 255 decimal.

## 8.2 Slot format

The data transmission format for each data value transmitted are as shown in table 5. Note that no parity is transmitted.

**Table 5 - Data Slot Format**

Bit Position	Description
1	Start Bit, Low or SPACE
2 through 9	Slot Value Data Bits, Least Significant Bit to Most Significant Bit
10, 11	Stop Bits, High or MARK

## 8.3 Break

The BREAK indicates the start of a new packet.

The BREAK generated by a transmitter is defined as a mark-to-space transition followed by a low of at least the minimum duration shown in table 6 (Timing Diagram, Designation #1) followed by a low to high transition.

Table 7 (Timing Diagram, Designation 1) defines the minimum duration break a receiver is required to recognize as the start of a new packet.

## 8.4 Mark after break

The MARK separating the BREAK and the START Code (Timing Diagram, Designation #2) is defined as the MARK AFTER BREAK. DMX512 transmitters produce a MARK AFTER BREAK that complies with the minimum and maximum values for designator 2 in table 6. Compliant receivers correctly respond to data streams with a MARK AFTER BREAK at least as long as the minimum shown in table 7.

*Note: The 1986 version of this Standard specified a 4 microsecond MARK AFTER BREAK. The 1990 version of the standard changed that value to 8 microseconds, but added an option for receivers capable of recognizing the 4 microsecond MARK AFTER BREAK to be identified as having that capability. Some transmitters may still be in use that generate the shorter 4 microsecond MARK AFTER BREAK, and they may not work with equipment built to this Standard.*

## 8.5 START code

The START Code is the first slot (slot 0) following a MARK AFTER BREAK. The START Code identifies the function of subsequent data in that packet.

### 8.5.1 NULL START code

A NULL START Code identifies subsequent data slots as a block of un-typed sequential 8-bit information. Packets identified by a NULL START Code are the default packets sent on DMX512 networks. Earlier versions of this Standard assumed that only dimmer class data would be sent using NULL START Code packets. In practice NULL START Code packets have been used by a wide variety of devices; this version recognizes this fact.

Each NULL START Code packet contains no formal data or addressing structure. The device using data from the packet must know the position of that data within the packet.

There is no guarantee that all NULL START Code packets will be delivered to all devices. Data sent using NULL START Codes should be of a type where loss of packet does not greatly affect the operation of the device. Hence data sent should be of the current value of a parameter, not a command to execute a routine. Once a controller is configured for a particular application, all NULL START Code packets should have the same number of slots.

### 8.5.2 Dimmer class data

Dimmer level data should be sent in NULL START Code packets. Valid dimmer levels shall be 0 to 255 decimal (00 to FF hexadecimal) representing dimmer control input. Value 0 shall represent a dimmer output of OFF or minimum and 255 shall represent an output of FULL. A dimmer shall respond to increasing the DMX512 slot value for 0 to 255 by fading from its minimum level (off) to its maximum level (full). The exact relationship between DMX512 slot values and dimmer output is beyond the scope of this Standard.

Note that NULL START Code packets are the default packets sent over DMX512 networks and may contain data other than dimmer class data.

### 8.5.3 Other START codes

In order to provide for future expansion and flexibility, DMX512 makes provision for 255 additional non NULL START Codes (1 through 255 decimal, 01 through FF hexadecimal), henceforth referred to as Alternate START Codes. Where it is required to send proprietary information over a DMX512 data link, a packet starting with a registered Alternate START Code shall be used.

Several Alternate START Codes are reserved. See Annex D.

See Annex E for Alternate START Code Registration Policies.

#### 8.5.3.1 Alternate START code refresh interval

A DMX512 transmitter interleaving NULL START Code packets with Alternate START Code packets shall send a NULL START Code packet at least once per second.

#### 8.5.3.2 Timing differences for Alternate START code packets

To ensure that in-line processing devices do not lose essential Alternate START Code data, a reduction of the maximum Alternate START Code update rate is necessary. One of the following methods shall be used:

- 1) Alternate START Code packets may be transmitted slower than the minimum timings specified in clause 8.11 by increasing the break to break time to 10% more than the minimum required for the Alternate START Code packets number of slots.
- 2) Transmitters may interlace non essential NULL START Code packets with Alternate START Code packets.

#### 8.5.3.3 Handling of Alternate START code packets by in-line devices

DMX512 processing devices or any device that receives and re-transmits DMX512 shall state in the manual for the product how they process Alternate START Code packets. The acceptable processing methods are:

- 1) Block all packets containing particular Alternate START Codes. The START Codes blocked shall be declared (and may be all Alternate START Codes).
- 2) Pass unmodified all packets containing particular Alternate START Codes. The START Codes passed shall be declared.
- 3) Process the information contained in packets containing particular Alternate START Codes. The algorithm shall be declared in enough detail to allow the user to decide if the device will satisfy their needs.

DMX512 in-line repeating transmitters shall not pass some packets with a particular Alternate START Code while blocking other packets containing the same Alternate START Code unless doing so as part of a stated processing algorithm.

### 8.5.4 START code processing

All receiving devices other than in-line processing devices shall process the START Code and differentiate between those packets with NULL START Codes and those with Alternate START Codes. Devices shall not

ignore START Codes by assuming that all packets received are NULL START Code packets.

#### **8.6 Maximum number of data slots**

Each data link shall support up to 512 data slots. Multiple links shall be used where larger numbers of slots are required.

#### **8.7 Minimum number of data slots**

There shall be no minimum number of data slots on the data link. DMX512 data packets with fewer than 512 slots may be transmitted, subject to the minimum timing requirements of this Standard – see clause 8.10 and figure 5.

#### **8.8 Defined line state between slots**

The time between any two slots of a data packet (Timing Diagram, Designation #9) may vary between minimum and maximum values shown for designator #9 of table 6. The line shall remain in a marking state during any such idle period.

#### **8.9 Defined line state between data packets (Mark Before Break)**

Every data packet transmitted on the data link, regardless of START Code or length, begins with a BREAK, MARK AFTER BREAK, and START Code sequence known as a Reset Sequence (Timing Diagram - Figure 5, Item 12). The time between the second stop bit of the last data slot of one data packet and the falling edge of the beginning of the BREAK for the next data packet (Timing Diagram, Designation #10) may vary between minimum and maximum values shown for designator #10 of table 6. The line shall remain in a marking state throughout any such period. Transmitters, therefore, shall not produce multiple BREAKs between data packets. Receivers, however, shall be capable of recovering from multiple BREAKs produced by data link line errors.

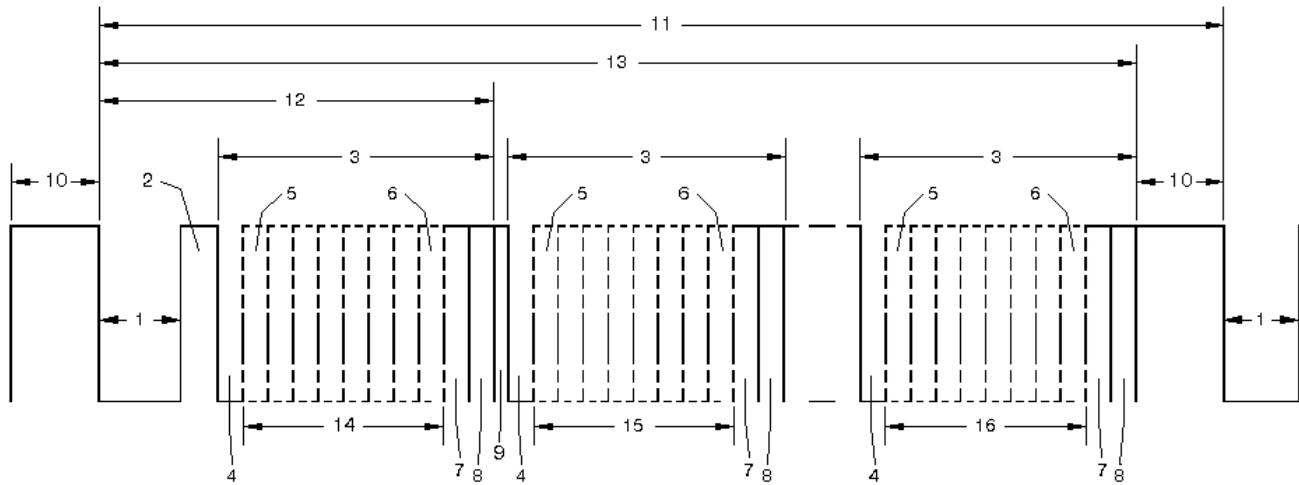
#### **8.10 Break-to-Break spacing**

Transmitters produce packets so that the period between the falling edge at the start of any one BREAK and the falling edge at the start of the next BREAK are not be less than the minimum value in table 6 designator #13. This period is also not more than the maximum value in table 6 designator #13.

Receivers operate correctly when receiving packets with break to break spacing of at least the minimum value in table 7 designator #13 up to the maximum value in table 7 designator #13.

#### **8.11 Timing Diagram - data+**

Timings shall follow the requirements of the timing diagram (figure 5) and its associated tables 6 and 7.



## Figure Key

- 1 - "SPACE" for BREAK
- 2 - "MARK" After BREAK (MAB)
- 3 - Slot Time
- 4 - START Bit
- 5 - LEAST SIGNIFICANT Data BIT
- 6 - MOST SIGNIFICANT Data BIT
- 7 - STOP Bit
- 8 - STOP Bit
- 9 - "MARK" Time Between slots
- 10- "MARK" Before BREAK (MBB)
- 11- BREAK to BREAK Time
- 12- RESET Sequence (BREAK, MAB, START Code)
- 13- DMX512 Packet
- 14- START CODE (SLOT 0 Data)
- 15- SLOT 1 DATA
- 16- SLOT nnn DATA (Maximum 512)

Figure 5 - Timing Diagram

**Table 6 - Timing Diagram Values - output of transmitting UART**

Designation	Description	Min	Typical	Max	Unit
-	Bit Rate	245	250	255	kbit / s
-	Bit Time	3.92	4	4.08	µs
-	Minimum Update Time for 513 slots	–	22.7	–	ms
-	Maximum Refresh Rate for 513 slots	–	44	–	updates / s
1	“SPACE” for BREAK	92	176	–	µs
2	“MARK” After BREAK (MAB)	12	–	< 1.00	µs s
9	“MARK” Time between slots	0	–	< 1.00	s
10	“MARK” Before BREAK (MBB)	0	–	< 1.00	s
11	BREAK to BREAK Time	1204	–	– 1.00	µs s
13	DMX512 Packet	1204	–	– 1.00	µs s

**Table 7 - Timing Diagram Values for Receivers**

Designation	Description	Min	Typical	Max	Unit
-	Bit Rate	245	250	255	kbit / s
-	Bit Time	3.92	4	4.08	µs
-	Minimum Update Time for 513 slots	–	22.7	–	ms
-	Maximum Refresh Rate for 513 slots	–	44	–	updates / s
1	“SPACE” for BREAK	88	176	–	µs
2	“MARK” After BREAK (MAB)	8	–	< 1.00	µs s
9	“MARK” Time between slots	0	–	< 1.00	s
10	“MARK” Before BREAK (MBB)	0	–	< 1.00	s
11	BREAK to BREAK Time	1196	–	– 1.25	µs s
13	DMX512 Packet	1196	–	– 1.25	µs s

*Note: Given the range of timing parameters shown in tables 6 and 7, a transmitter may produce a signal with a refresh rate in the range of 1 Hz to approximately 830 Hz. A receiver must be capable of accepting a signal with a refresh rate of 0.8 Hz to approximately 836 Hz.*

## 9 Receiver Performance

### 9.1 Rejection of Improperly framed slots

A receiver shall check the first stop bit and should check the second stop bit of all received slots to determine if they have the correct value. If a missing stop bit is detected, the receiver shall discard the improperly framed slot data and all following slots in the packet.



### 9.2 Loss of data tolerance / Resumption of acceptance of data

A receiver not receiving a Reset Sequence (a sequence of a Break, Mark After Break, and START Code) within one maximum break to break time (as per table 7) of the previous Reset Sequence is considered to have lost data input.

Although this Standard does not specify loss of data handling procedures, manufacturers shall state what their Loss of Data handling procedures are.

*Note: In the absence of overriding safety issues or an alternative source of control data, when encountering a loss of data condition a receiving device should remain in an operating condition for at least 60 seconds, awaiting resumption of the DMX512 signal.*

### 9.3 Receiver performance at maximum refresh rate

Any device incorporating a DMX512 receiver shall operate correctly when receiving continuous transmission of valid data packets containing any number of valid slot values.

### 9.4 Packet processing latency

Some products may provide their specified functionality without processing or being able to process every consecutive DMX512 packet. Such products will have an inherent latency to data changes between packets, which shall be declared by the manufacturer in accordance with the disclosure requirements of clause 10.

## 10 Marking and Disclosures

In this Standard, marking is defined as the application of a physical mark/label, etc. on the product, and declaration means declared in a manual and optionally marked on the product.

### 10.1 Identification

Only equipment conforming to this Standard may be marked and identified with "USITT DMX512-A" or "DMX512-A".

### 10.2 DMX512 port marking

Where required by clauses of this Standard, all DMX512 ports shall be marked as to the applicable Enhanced Functionality as defined in table B1 (Annex B). All information provided by marking shall also be provided in the equipment manual.

Manufacturers shall use the signal designations from table 3 in any pinout detail declaration or marking of pin, contact or terminal functions appearing on or within a product and associated with installation or connection. Where it is necessary to use abbreviations, only those detailed in table 8 shall be permitted.

**Table 8 - Signal designations abbreviations allowed for marking**

Function	Preferred Abbreviation	Non preferred Abbreviation
Common Reference	COM	C
Primary Data Link – Data 1-	D1-	1-
Primary Data Link – Data 1+	D1+	1+
Secondary Data Link – Data 2-	D2-	2-
Secondary Data Link – Data 2+	D2+	2+

### 10.3 Data line termination marking

Products that have switchable (in/out) termination circuits shall provide indication of the termination state.

#### 10.4 Ground / Isolation marking

All DMX512 ports shall indicate the relationship between Data Link Common and earth ground. The allowed grounding topologies are shown in table 9.

**Table 9 - Ground / Isolation marking**

Function of DMX512 port	Defining Clause / Figure	Comment	Approved Marking
Transmitter	clause 5.4 / fig 1	Ground Referenced	no mark required, recommended mark
Transmitter	clause A1 / fig A1	Isolated (See Annex A)	ISO or ISOLATED
Transmitter	clause A4 / fig A4	Floating (See Annex A)	FLT or FLOAT or FLOATING
Receiver	clause A2 / fig A2	Non-Isolated, 100 ohm 2 Watt resistor	NON-ISO or NON-ISOLATED
Receiver	clause A3 / fig A3	Grounded – concession per clause A3	
Receiver	clause 5.7 / fig 3	Isolated	<i>no mark required</i> ; ISO or ISOLATED
Receiver	clause A4 / fig A4	Floating	FLT or FLOAT or FLOATING

*Note: Although no mark is required of Ground Referenced transmitters or Isolated receivers, it is highly recommended that such markings appear on the product.*

#### 10.5 Required disclosures and markings

##### 10.5.1 Portable products and products fitted with external pluggable data link connectors

DMX512 ports on these products shall be marked in accordance with clause 10.2. DMX512 ports on these products shall provide Ground/Isolation marking in accordance with clause 10.4.

If use has been made of any non-XLR connector in conjunction with the supply of an adapter as permitted by clause 7.1.2, the non-XLR connector shall be declared in the equipment manual as NCC DMX512-A and also be marked (when feasible) in accordance with that clause.

##### 10.5.2 Equipment intended for fixed installation with internal connections to the data link

DMX512 ports on these products shall be marked in accordance with clause 10.2. DMX512 ports on these products shall provide Ground/Isolation marking in accordance with clause 10.4.

Clearly identified terminal contact (connector pinout) detail shall be marked on or within any product in accordance with clause 10.2.

##### 10.5.3 Loss of data handling procedure

This Standard does not define loss of data handling procedures (clause 9) beyond requiring that manufacturers declare their own products' procedure(s). Such declarations shall be made in the equipment manual.

##### 10.5.4 Packet processing latency

Manufacturers of in-line DMX512 processing, or distribution devices, shall declare any inherent latency in the processing of data packets, including a statement of the worst case delay between receiving a packet and that packet affecting the product's output. A statement of the worst case percentage number of zero start code packets that are discarded by the product shall also be included.

##### 10.5.5 NULL START Code functionality

Manufacturers of transmitting devices shall declare in the equipment manual the full range of slot values transmitted in conjunction with packets sent using the NULL START Code.

Manufacturers of receiving devices shall declare the response to packets received containing the NULL START Code, with particular reference to any functionality requiring limited or restricted slot data values.

**10.5.6 Slot footprint**

Manufacturers of receiving devices shall declare the slot footprint in the equipment manual.

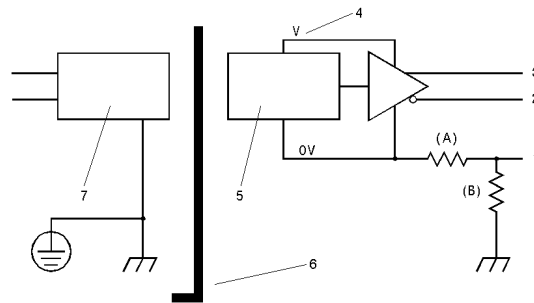
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## Annex A - Non Preferred (Alternate) topologies (Normative)

### A1 Isolated transmitters

This standard permits the use of isolated transmitter ports. They are used in legacy systems where grounded receivers are used and large Common Mode voltages are expected.

Figure A1 illustrates an isolated transmitter port. To be considered an isolated transmitter, any signal pin or contact of the DMX512 output shall present a resistance (B) greater than 22 Mohm at 42 VDC with respect to Chassis, and with respect to Protective Ground (where fitted). If there are any other signal inputs or outputs, any signal pin or contact of the DMX512 output shall present a resistance greater than 22 Mohm at 42 VDC with respect to these inputs or outputs. The power supply for the transmitter and any directly connected electronics shall be isolated from earth ground and any other grounded referenced electronics to levels at least as high as those required of the output. Any resistance (A) between Data Link Common's pin or contact and zero volt supply (circuit common) of the transmitter circuit shall be less than 100 ohms. There may be a capacitance (not shown) between Data Link Common and chassis for the purpose of Radio Frequency bypass.



#### Figure Key

- 1 - DMX512 Data Link Common
- 2 - DMX512 Data 1- (or Data 2-)
- 3 - DMX512 Data 1+(or Data 2+)
- 4 - V (+ or -)
- 5 - Other Isolated Electronics
- 6 - Isolation Barrier
- 7 - Non-Isolated Electronics (optional)
- A - Optional resistance (see text)
- B - Resistance (see text)

Figure A1 - Isolated Transmitter

**Table A1 - Isolated Transmitter characteristics**

Connection	Limit (measured at port pin or contact)	Comment
Data 1- to Data Link Common or Data 1+ to Data Link Common	+/- 6 V	Common Mode range
Data 2- to Data Link Common or Data 2+ to Data Link Common	+/- 6 V	Enhanced Function devices only
Data Link Common to Chassis	> 22M ohm @ 42 VDC	
Data 1- to Chassis or Data 1+ to Chassis	> 22M ohm @ 42 VDC	
Data 2- to Chassis or Data 2+ to Chassis	> 22M ohm @ 42 VDC	Enhanced Function devices only
Data 1- to Data 1+	+/- 6 V	
Data 2- to Data 2+	+/- 6 V	Enhanced Function devices only
Any Port Pin or Contact to Chassis	30 VAC / 42 VDC	

A DMX512 device may have any number of isolated transmitter ports.

Adherence to this topology allows a DMX512 transmitter connector to be marked ISO or ISOLATED.

### A2 Non-isolated receivers

While not the preferred topology, this non-isolated topology exhibits considerable improvement in common mode fault tolerance compared to other grounded or non-isolated topologies. In this topology there shall be a resistance (B) of 100 ohms between Data Link Common's pin or contact and chassis. This resistance shall be able to safely dissipate two watts. No other connection between data link common and chassis is permitted. Common Mode voltage present between the chassis of this device and the chassis of any other device connected to the DMX512 shield will cause a current flow. This current will cause a voltage drop in the resistance (B). This voltage drop effectively decreases the Common Mode voltage at this receiver. Any resistance (A) between Data Link Common's pin or contact and zero volt supply (circuit common) of the receiver circuit shall be less than 100 ohms.

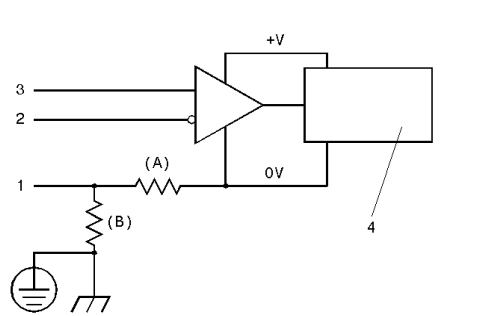


Figure Key

- 1 - DMX512 Data Link Common
- 2 - DMX512 Data 1- (or Data 2-)
- 3 - DMX512 Data 1+ (or Data 2+)
- 4 - Other Electronics
- A - Optional resistance (see text)
- B - Optional resistance (see text)

Figure A2 - Non-Isolated Receiver

Since 0 V is not directly referenced to Chassis, local product safety standards may restrict choice of power supply (e.g., use of a Class 2 supply).

A DMX512 receiver may have any number of non-isolated receiver ports. Where multiple ports are implemented, the total parallel resistance (B) shall be 100 ohms.

**Table A2 - Non-Isolated Receiver characteristics**

Connection	Limit	Comment
Data 1- to Data Link Common or Data 1+ to Data Link Common	+12 / -7 VDC	Common Mode range
Data 2- to Data Link Common or Data 2+ to Data Link Common	+12 / -7 VDC	Enhanced Function devices only
Data Link Common to Chassis	100 ohms	-Note 1-
Data 1- to Chassis or Data 1+ to Chassis	+12 / -7 VDC	
Data 2- to Chassis or Data 2+ to Chassis	+12 / -7 VDC	Enhanced Function devices only
Data 1- to Data 1+	+/- 6V	
Data 2- to Data 2+	+/- 6V	Enhanced Function devices only
Any Port Pin or Contact to Chassis	N/A	

*Note 1: This cannot be characterized in terms of voltage.*

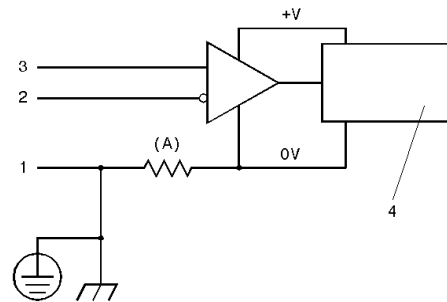
Manufacturers shall be permitted to fit a resistance of 100 ohms +/-20% between Chassis and Data Link Common for the purpose of limiting current in the shield due to small differential ground potentials. This method provides for reduction of Common Mode voltage at the line receiver.

The only output that shall be permitted to be directly connected to this topology is a single passive DMX512 loop through port. No other inputs or outputs are allowed with this topology unless they meet the requirements of clause A4.

### **A3 Grounded Receivers**

The topology of Figure A3 is allowed for the construction of entry level receivers where the cost of isolation might prove an untenable burden. It may be used by manufacturers of receivers who, for reasons beyond the scope of this Standard require a direct link between data link common and protective earth. It is not a recommended practice and requires special marking on the product and special explanatory text in all manuals.

This topology is characterized by the direct connection of the shield (Data Link Common) to chassis and protective earth. Therefore, devices employing ground referenced receivers shall be provided with a connection to protective earth. Any resistance (A) between Data Link Common's pin or contact and zero volt supply (circuit common) of the receiver circuit shall be less than 100 ohms.



## Figure Key

- 1 - DMX512 Data Link Common
- 2 - DMX512 Data 1- (or Data 2- )
- 3 - DMX512 Data 1+ (or Data 2+ )
- 4 - Other Electronics
- A - Optional Resistance (see text)

Figure A3 - Grounded Receiver

Ports using this topology shall be marked using the standard symbol representation as defined in clause 10.5 and be declared.

#### A4 Earth grounding of data link common for floating devices

Figure A4 illustrates a floating topology. Floating is both an input and an output topology and is an additional allowable topology. It is often confused with the isolated DMX512 topology. As with the isolated topology, any input or output signal pin or contact shall present a resistance (B) greater than 22 Mohm at 42 VDC with respect to Chassis, and with respect to Protective Ground (where fitted). It differs from an isolated topology in that there is no requirement of isolation between DMX512 inputs and outputs. The resistance between Data Link Common's pin or contact of the DMX512 input and Data Link Common's pin or contact of the DMX512 output shall be less than 0.2 ohms. There may be a capacitance (not shown) between Data Link Common and chassis for the purpose of Radio Frequency bypass. Any resistance (A) between any Data Link Common's pin or contact and the zero volt supply (circuit common) of the transmitter and receiver circuits shall be less than 100 ohms.

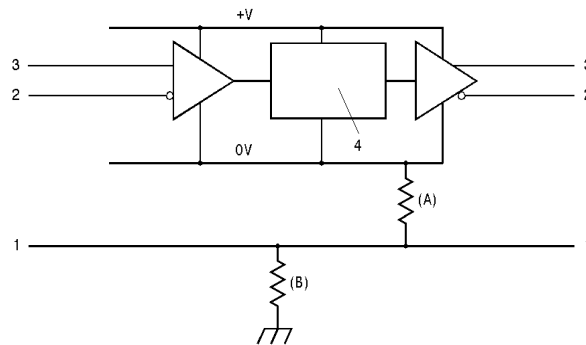


Figure A4 - DMX512 Device, Floating

The grounding of a device using this topology is determined by the connected devices. For that reason this topology shall not be used for devices that provide ground referenced non-DMX512 input or output ports unless those ports are isolated from DMX512 lines by an impedance of at least 22 Mohms.

Both input and output ports of a floating device shall be marked FLT, FLOAT, or FLOATING. A device may have only one floating DMX512 receiver port.

*-end of Annex A-*



## Annex B (Normative) - Enhanced DMX512

### B1 General

The original and 1990 versions of USITT DMX512 called out an “Optional Second Data Link.” There was no detailed guidance for its use. The majority of legacy systems did not use the second data link at all. Many uses of the second data link have been implemented over the years. While many of these were reasonable, a few uses clearly were not compliant with EIA-485-A. These uses vary in both their electrical requirements and in the data protocol used. One of the purposes of this Standard is to regularize the use of the second data link. It is no longer possible to select a single implementation and forbid all others. However, not all historical uses will be allowed to continue.

The network topologies needed to support Enhanced Functions are identified by an EF number. This edition of the standard supports four different EF topologies.

The introduction of standard EF topologies in no way changes backward compatibility of primary data link functions. In all cases, regardless of the EF topology, all DMX512 transmitters and receivers shall be able to interchange DMX512 data on the primary data link. All DMX512 devices shall be able to be connected without damage. All DMX512 devices shall not be damaged by connection to compliant legacy devices.

A DMX512 controlled device capable of returning status information is referred to as a responder in this Standard. For the purposes of this Standard, responders are not considered to fall under the category of transmitting devices.

### B2 Summary of Enhanced Function Topologies

The Enhanced Function topologies are summarized in table B1. The data format on primary data link (Data 1- and Data 1+) shall adhere to the DMX512-A Standard

**Table B1 - Enhanced Function topologies**

EF #	Symbol (Optional)	Description	Comment
1	↔ —	half duplex EIA-485-A signals on primary data link; return signals on primary data link controlled by a registered Alternate START Code; no functionality on secondary data link	
2	→ ←	unidirectional DMX512 data on primary data link (EIA-485-A signals) and return EIA-485-A signals on secondary data link	
3	→ ↔	unidirectional DMX512 data on primary data link (EIA-485-A signals) and half duplex EIA-485-A signals on secondary data link	refer to manufacturers instructions
4	↔ ↔	half duplex EIA-485-A signals on both pairs; return signal on primary data link controlled by a registered Alternate START Code	

*Note: References to unidirectional data are with respect to a transmitting device.*

Different physical DMX512 ports on a product may be of different EF topologies and shall be declared and marked as required in clause 10.

### B3 Identification of data protocols for Enhanced DMX512

The EF topology specifies the electrical and operating mode for the data links. It does not detail the data structure or protocol. The method of identifying data structures or protocols using the defined EF numbers is by way of an additional registered number placed after the EF number, separated from the EF number by a period. The registry for these designations will be maintained by Secretariat for the ANSI E1 Accredited Standards

Committee – ESTA (see Annexes D and E). Numbers ending in zero are reserved for future development of the standard (e.g., EF1.0, EF1.10, EF2.20).

### **B3.1 EF1 Half Duplex DMX512 - Bidirectional use of the primary data link**

Systems that send data in both directions on the primary data link are classified as EF1. These systems shall use the primary data link for both the NULL START Code DMX512 signal packets as well as return data controlled by the use of Alternate START Code packets. There is no specific requirement that EF1 devices use NULL START Code packets for any of their functions – that requirement is defined by the specific EF protocol.

An EF1 system shall use polled responses on the primary data link, such that a receiving device can not transmit a packet unless instructed to by an appropriate Alternate START Code packet from the controller. All response packets shall begin with an Alternate START Code. Once configured, any functions using EF1 shall use collision free data protocols.

All packets in an EF1 system shall follow the normal timing and limits for a DMX512 packet. There may be additional timing limits imposed by the chosen protocol. Any additional timing limits are beyond the scope of this Standard.

#### **B3.1.1 Bi-directional distribution amplifiers for EF1**

Systems using EF1 topologies require bi-directional distribution/return data combiners. These combiners shall control the direction of data flow on the primary data link. The design of such a bi-directional distribution/return data combiner requires detailed understanding of the protocol timings. Therefore, the design of bi-directional distribution/return data combiners for EF1 without knowledge of the protocol to be used is meaningless. The requirements for such designs are beyond the scope of this Standard.

#### **B3.1.2 Termination of EF1 system**

Termination of EF1 primary data links shall conform to the electrical requirements clause 4.9. Additionally, EF1 systems shall terminate each end of the primary data link. Therefore, EF1 controllers and other transmitting devices shall provide a means to terminate the primary data link. Such terminations may also require specific line biasing or other methods to ensure integrity of returned data that are beyond the scope of this Standard.

### **B3.2 EF2 - Full duplex DMX512**

The EF2 topology uses the second data link to provide a data path to return information from controlled devices. The data on second data link shall be unidirectional flowing from the controlled devices to the controller. This data link will operate in multi transmitter multipoint mode. In this mode the primary and secondary links comprise a full duplex data link.

Each responder shall have an EIA-485-A transmitter for the second data link with a driver enable control. The driver enable control shall be driven so that each responder can control the state of the return data link while transmitting its response bytes. Once configured only one responder shall be enabled at once and there shall be at least one bit time between one responder going inactive and the next going active. In general, the line driver can be enabled one bit time prior to transmission, and disabled one bit time after the last bit has been sent.

Once configured, any functions using EF2 shall use collision free data protocols. EF2 protocols shall also be structured to allow the use of data distribution amplifiers that meet the requirements of clause B3.2.2.

#### **B3.2.1 Wiring of EF2 DMX512 ports**

EF2 responders having two DMX512 ports for receive and transmit shall provide a direct passive link for Data 2- and Data 2+ between those ports (clause 4.8.2). The responder transmitter shall be connected to this passive link. Devices having three or more DMX512 ports shall wire the additional ports in a manner appropriate for the device's functionality. The manner in which these ports are wired shall be clearly detailed in the product's manual. Devices having three or more ports shall have two ports wired as a loop through with an attached

responder transmitter.

### **B3.2.2 Bi-directional distribution amplifiers for EF2**

Systems using EF2 topologies require bi-directional distribution amplifiers/return data combiners. The DMX512 primary data link may be split and separately buffered as in standard DMX512 buffers. Return data receivers shall be "wire-OR" connected within a unit. This combined received data signal is used to drive back to the return data monitor.

The bi-directional distribution amplifier shall not perform any processing on the data, since some response protocols depend upon the relationship with outbound DMX512 to synchronize the return data.

### **B3.2.3 Termination of EF2 data links**

EF2 systems shall terminate the primary data link following the requirements of section 4.9. They shall also terminate the secondary data link to conform to the electrical requirements of 4.9 except that both ends of the secondary data link shall be terminated. Therefore, EF2 controllers and other transmitting devices shall provide a means to terminate the secondary data link. Such terminations may also require specific line biasing or other methods to ensure integrity of returned data that are beyond the scope of this Standard.

### **B3.3 EF3 Half duplex on the second data link**

Systems that send data in both directions on the secondary data link are classified as EF3. These systems shall use the primary data link to send a standard unidirectional DMX512 signal.

#### **B3.3.1 Bi-directional distribution amplifiers for EF3**

Systems using EF3 topologies require bi-directional distribution/return data combiners. These combiners shall control the direction of data flow on the secondary data link. The design of such a bi-directional distribution/return data combiners requires detailed understanding of the protocol timings. Therefore, the design of bi-directional distribution/return data combiners for EF3 without knowledge of the protocol to be used is meaningless. The requirements for such designs are beyond the scope of this Standard.

#### **B3.3.2 Termination of EF3 data links**

EF3 systems shall terminate the primary data link following the requirements of clause 4.9. They shall also terminate the secondary data link to conform to the electrical requirements of 4.9 except that both ends of the secondary data link shall be terminated. Therefore, EF3 controllers and other transmitting devices shall provide a means to terminate the secondary data link. Such terminations may also require specific line biasing or other methods to ensure integrity of returned data that are beyond the scope of this Standard.

### **B3.4 EF4 Protocols that use the primary and the secondary data links in ways not covered above**

Systems that use the primary and the secondary data links to send data in both directions are classified as EF4. Both data links shall comply with the requirements of clauses B3.1 (EF1) and fall within the scope of EIA-485-A except that the use of the secondary data link is optional.

### **B3.5 Additional electrical requirements**

The details of a particular protocol using an EF topology may necessitate additional electrical requirements. These requirements are beyond the scope of this document.

*-end of Annex B-*

**Annex C (Normative) - Higher Protection Levels – “DMX512-A Protected”**

Some manufacturers feel it is prudent to employ higher levels of protection on their DMX512 ports than is specified in EIA-485-A. Many semiconductor manufacturers have recognized the need for higher protection and have produced “fault protected transceivers.” The tables below indicate the minimum requirements for a protected DMX512 port. If a manufacturer’s DMX512 port meets these requirements, the port can be declared as “DMX512-A Protected”.

**Table C1 - Transmitter protection**

Connection	Minimum Protection Limit		
Data 1- to Data Link Common or Data 1+ to Data Link Common	30 VAC / ± 42 VDC		
Data 2- to Data Link Common or Data 2+ to Data Link Common	30 VAC / ± 42 VDC		
Data 1- to Data 1+	30 VAC / ± 42 VDC		
Data 2- to Data 2+	30 VAC / ± 42 VDC		
	Ground Referenced	Isolated	Floating
Data Link Common to Chassis	< 0.2 ohms	N/A	N/A
Any other non Data Link Common Port Pin or contact to Chassis	30 VAC / ± 42 VDC	N/A	N/A
Any Port Pin or Contact to Chassis	N/A	30 VAC / ± 42 VDC	30 VAC / ± 42 VDC

**Table C2 - Receiver protection**

Connection	Minimum Protection Limit		
Data 1- to Data Link Common or Data 1+ to Data Link Common	30 VAC / ± 42 VDC		
Data 2- to Data Link Common or Data 2+ to Data Link Common	30 VAC / ± 42 VDC		
Data 1- to Data 1+	30 VAC / ± 42 VDC		
Data 2- to Data 2+	30 VAC / ± 42 VDC		
	Non-Isolated	Isolated	Floating
Data Link Common to Chassis	-note 1-	N/A	N/A
Any other non Data Link Common Port Pin or contact to Chassis	30 VAC / ± 42 VDC	N/A	N/A
Any Port Pin or Contact to Chassis	N/A	30 VAC / ± 42 VDC 100Mohm at 50 VDC	30 VAC / ± 42 VDC > 22Mohm at 50 VDC

*Note 1: This cannot be characterized in terms of voltage. Clause A2 (Receiver Characteristics) allows manufacturers to fit a resistance between chassis and Data Link Common for the purpose of limiting the current in the shield due to small ground differentials. Any such resistance shall survive continuous connection to voltages within the EIA-485 Common Mode range of -7/+12 VDC.*

-end of Annex C-

## Annex D (Normative) - Reserved Alternate START Codes

### D1 Reserved Alternate START Codes

Several Alternate START Codes are reserved for special purposes or for future development of the Standard. No equipment shall be manufactured that generates Alternate START Codes 92 - A9 (146 - 169 decimal) or AB - CD (171 - 205 decimal) until their use is defined by the Standard or by the E1 Accredited Standards Committee. Manufacturers shall not advertise or sell products or devices that use Alternate START Codes F0 - F7 (240 - 247 decimal).

**Table D1 - Reserved Alternate START Codes**

Alternate START Code		Purpose	Note
Hexadecimal	Decimal		
17	23	ASCII Text Packet	see Annex Clause D2 for implementation
55	85	Test Packet	see Annex Clause D3 for implementation
90	144	UTF-8 Text Packet	see Annex Clause D4 for implementation
91	145	91h followed by a 2 byte Manufacturer ID field is reserved for Manufacturer/Organization specific use, transmitted byte order is MSB, LSB. The next byte after the Manufacturers ID would normally be a manufacturer's sub-code	The Manufacturer ID serves as an identifier that the data following in that packet is proprietary to that entity and should be ignored by all others
92 - A9	146 - 169	possible future revisions of this Standard	Use not currently permitted
AB - CD	171 - 205	possible future revisions of this Standard	Use not currently permitted
CF	207	System Information Packet	see Annex clause D5 for implementation
F0 - F7	240 - 247	prototyping/experimental use while the manufacturer/organization is waiting for their registered Alternate START Code to be assigned	Not permitted in shipping product

### D2 ASC text packet

Alternate START Code 17h (23 decimal) shall designate a special packet of between 3 and 512 data slots. The purpose of the ASCII text packet is to allow equipment to send diagnostic information coded per the American Standard Code for Information Interchange and formatted for display.

Slot allocation is as follows:

Slot 1: Page number of one of the possible 256 text pages.

Slot 2: Characters per Line. Indicates the number of characters per line that the transmitting device has used for the purposes of formatting the text. A slot value of zero indicates ignore this field.

Slots 3-512: Consecutive display characters in ASCII format. All characters are allowed and where a DMX512 text viewer is capable, it shall display the data using the ISO/IEC 646 standard character set. A slot value of zero shall terminate the ASCII string. Slots transmitted after this null terminator up to the reset sequence shall be ignored.

### D3 ASC test packet

Alternate START Code 55h (85 decimal) shall designate a special test packet of 512 data slots, where all data slots carry the value 55h (85 decimal). Test packets shall be sent so that the time from the start of the Break until the stop bit of the 513<sup>th</sup> slot shall be no more than 25 milliseconds. When test packets are sent back to back, the Mark Before Break time shall be no more than 88 microseconds. The Break timing for test packets shall be greater than or equal to 88 microseconds, and less than or equal to 120 microseconds. The Mark After Break time shall be greater than or equal to 8 microseconds and less than or equal to 16 microseconds.

### D4 UTF-8 text packet

Alternate START Code 90h (144 decimal) shall designate a special packet of between 3 and 512 data slots. The purpose of the UTF-8 Text Packet is to allow equipment to send diagnostic information coded per UTF-8 as described in Unicode 5.0 published by The Unicode Consortium and formatted for display. UTF-8 should only be used when the text packet cannot be expressed in ASCII per clause D2.

Slot allocation is as follows:

Slot 1: Page number of one of the possible 256 text pages.

Slot 2: Characters per Line. Indicates the number of characters per line that the transmitting device has used for the purposes of formatting the text. A slot value of zero indicates "Ignore this field."

Slots 3 - 512: Consecutive display characters in UTF-8 format. All characters are allowed and where a DMX512 text viewer is capable, it shall display the data using the Unicode 5.0 character set. A slot value of zero shall terminate the UTF-8 text string. Slots transmitted after this null terminator up to the reset sequence shall be ignored.

### D5 System Information Packet (SIP) Alternate START Code

Alternate START Code CFh (207 decimal) is reserved for a System Information Packet (SIP). The SIP includes a method of sending checksum data relating to the previous NULL START Code packet on the data link and other control information. No other packet shall be sent between the NULL START Code packet and the SIP that carries its checksum.

#### D5.1 Application

Manufacturers of control consoles are encouraged to transmit SIPs, either as a background to normal processing or, in conjunction with the special test packet, as part of their suite of system test functions. One of the current problems with testing of DMX512 installations is that it must be done with static test packets – certain modes of testers cannot be used while a console is actually running the show, as by definition the DMX512 packets are varying as each cue runs. The interleaving of SIP's would allow some degree of live testing, particularly if one of more test packets were also sent applicable to the functionality of the receiving device.

*Note: For systems requiring a more reliable link, manufacturers would have the option of following every normal packet with a SIP packet, although it is recognized that this would degrade data throughput. It could be used with systems that send packets of fewer than 512 DMX512 data slots or refresh data at less than the maximum rate.*

#### D5.2 SIP format

The SIP Packet Length is 24 data slots, in the format specified in Table D2. Receivers shall be required to accept SIPs of up to 255 data slots to allow for future expansion.

**D5.3 SIP checksum pointer**

Transmitting devices shall send a value of 24 in slot 1 that represents the length of SIP Packet in this version of the Standard. Receivers shall use the value received in slot 1 to establish the offset to the SIP checksum.

**Table D2 - SIP Format**

Slot	Definition	Refer to Clause
1	SIP Byte Count/SIP Checksum pointer (valid value is 24)	D5.3
2	Control Bit Field	D5.4
3	MSB of 16 bit additive Checksum of previous packet	D5.5
4	LSB of the 16 bit Checksum of previous packet	D5.5
5	SIP sequence number	D5.6
6	DMX512 universe number	D5.7
7	DMX512 processing level	D5.8
8	Version of Software sending this SIP	D5.9
9	Standard Packet Len MSB	
10	Standard Packet Len LSB	D5.10
11	Number of Packets transmitted by originating device since last SIP MSB	
12	Number of Packets transmitted by originating device since last SIP LSB	
13	Originating Device's Manufacturer ID MSB	D5.11
14	Originating Device's Manufacturer ID LSB	D5.12
15	Second Device's Manufacturer ID MSB	D5.13
16	Second Device's Manufacturer ID LSB	D5.13
17	3 <sup>rd</sup> Device's Manufacturer ID MSB	D5.13
18	3 <sup>rd</sup> Device's Manufacturer ID LSB	D5.13
19	4 <sup>th</sup> Device's Manufacturer ID MSB	D5.13
20	4 <sup>th</sup> Device's Manufacturer ID LSB	D5.13
21	5 <sup>th</sup> Device's Manufacturer ID MSB	D5.13
22	5 <sup>th</sup> Device's Manufacturer ID LSB	D5.13
23	<i>reserved for future use - transmit as 0</i>	
24 - (nn-1)	<i>reserved for future use</i>	D5.3
nn (max 255)	8-bit Additive Checksum of the SIP	D5.14

**D5.4 Control bit field**

d7	d6	d5	d4	d3	d2	d1	d0
reserved transmit as 0	reserved transmit as 0	reserved transmit as 0	reserved transmit as 0	reserved transmit as 0	reserved transmit as 0	previous packet bit set = 1	subsequent NULL packet hold control bit set=1

**D5.4.1 Subsequent NULL packet hold control bit d0**

Processing of the subsequent NULL packet hold Control Bit is optional. If implemented, when the subsequent NULL packet hold Control Bit is set (=1), the subsequent NULL START Code packet shall be held pending the reception of the next SIP for validation of the checksum. If a second NULL START Code packet is received without a preceding SIP, the receiver shall return to an immediate use mode.

**D5.4.2 Previous packet bit d1**

Set (= 1) if previous packet was an Alternate Start Code (ASC) packet.

**D5.5 Checksums**

16 bit ones complement additive checksum of all slots in the previous packet. The checksum includes the START Code.

**D5.6 SIP Sequence number**

A free running 8 bit counter identifying the SIP and incremented by a SIP generator by 01h on every subsequent SIP. This field may be checked to ensure that SIPs have not been missed.

**D5.7 Originating universe**

This slot indicates the (originating) DMX512 universe currently transmitted on this link. 00h is not used. Valid values 01h - FFh (1 decimal - 255 decimal).

**D5.8 DMX512 processing level**

This slot indicates the level of post controller processing. Originating devices shall always transmit a value of 00h in this field. Processing devices such as merge units or any that regenerate or provide a media conversion (e.g., Ethernet to DMX512) facility and do not explicitly block ASC test packets per clause D3 shall increment the value of this field by 01h. The content of this field indicates a level of process "hops" that data on the link has been subjected to relative to the originating transmitting device.

**D5.9 Software version**

00h not implemented  
01h - FFh firmware version of last device

*Note: This slot for use by the manufacturer and may not correlate with any formally published release identifier.*

**D5.10 Packet lengths**

This declares the standard length of packets for START Code 00, normally transmitted on this link. Valid values are

0000h	packet length not declared
0001h - 0200h	designates value of fixed packet length
0201h - 7FFFh	are reserved
8000h	Dynamic Packet, length not declared
8001h - 8200h	length of last dynamic packet
8201h - FFFFh	are reserved

**D5.11 Number of packets**

A 16 bit count of the number of packets transmitted by the originating device since last SIP was transmitted. This count should not increment past FFFFh.

**D5.12 Manufacturer ID**

Manufacturer ID will be the same 16 bit assignment as used for the Manufacturer's ID field used with Alternate START Code 91h (see Annex E - clause E1).



an ID == 0000h indicates that Manufacturer is not declared.

an ID == FFFFh indicates that Manufacturer has applied for, but not been granted, and ID and that this transmission originates from a product under development.

#### **D5.13 Packet history**

DMX512 Processing devices and media converters that process SIPs shall be required to insert their own Manufacturer's ID into the SIP packet. An originating device shall always send its Manufacturer's ID in SIP slots 13 and 14, with 0000h in slots 15, 16; 17, 18; 19, 20 and 21, 22. Subsequent processing devices shall insert their manufacturer's ID into the slots as indicated by the DMX512 processing level slot. A processing level of 01h corresponds to the second device, a processing level of 02h corresponds to the third device, and so on.

*Note: This scheme allows for a packet processing history to be traced back though a complex installation of products.*

#### **D5.14 SIP Checksum**

8 bit ones complement additive checksum of the SIP START Code (CFh) and all subsequent slots of SIP data.

*-end of Annex D-*

**Annex E (Normative) - Alternate START Code, Manufacturer ID, and Enhanced Functionality Registration****E1 Alternate START Code Registration Policy: 1 - 255 decimal (01 - FF hexadecimal)**

Slot 0 of a DMX512 packet is the START Code. The value of this slot identifies intended use of data in the rest of the packet. The Standard provides for a non NULL or "Alternate" START Code. Where it is required to send proprietary information over a DMX512 data link, a packet starting with a registered Alternate START Code shall be used.

**E2 Authorized use**

The E1 Accredited Standards Committee or any organization that it authorizes may use an Alternate START Code to provide further extensions to the DMX512 Standard.

**E3 Reserved Alternate START Codes**

Several Alternate START Codes are reserved for special purposes or for future development of the Standard. See Annex D.

**E4 Requests for Registration of New START Codes**

Any manufacturer or organizations involved in the use of DMX512 may request that a START Code or Manufacturer ID be registered for their use. Although not encouraged, an Alternate START Code and Manufacturer ID may be registered for proprietary use. Requests shall be forwarded to the Secretariat for the ANSI E1 Accredited Standards Committee – ESTA. ESTA will attempt to honor such reasonable requests as described below.

**E4.1 Number of Alternate START Codes per entity**

No more than one Alternate START Code may be registered to any one manufacturer/organization. Manufacturers and Organizations with Alternate START Codes registered prior to the publication of this Standard may request one additional Alternate START Code.

**E4.2 Selection of the Alternate START Code value and Manufacturer ID**

The assignment of any particular numeric START Code or Manufacturer ID value to any particular entity is solely at the discretion of Accredited Standards Committee E1. Assignment depends on the availability of unused and unreserved START Codes and Manufacturer IDs.

**E5 Requirements for registration of an EF protocol**

No EF protocol intended for use between multiple Manufacturer's will be registered as an EF protocol unless its basic structure is available to anyone by request and can be used freely by any manufacturer. The entire message structure for the protocol does not have to be made public, only the portions that are for public use. It is expected that some protocols may still have portions of the message structure that are reserved for proprietary use (i.e., vendor specific messages). Registration is at the discretion of Accredited Standards Committee E1.

**E6 Documentation Register****E6.1 Documentation for use of Alternate START Codes**

The manufacturer/organization requesting registration of an Alternate START Code shall provide a 2-line description of the purpose of the Alternate START Code. They shall list the minimum and maximum number of slots, including the START Code, in any proposed packet. Any provided description (subject to editing) shall be included in the Register. This is not required for functions associated with a manufacturer specific ID under Alternate START Code 91. It is recommended, but not required, for Alternate START Codes assigned prior to the adoption of this version of the Standard.

**E6.2 Maintenance and Publication**

The ANSI E1 Accredited Standards Committee through its secretariat (ESTA) shall maintain a Register of

Alternate START Codes and Manufacturer IDs. ESTA will publish the Registry as needed.

**E6.3 Supplemental documentation**

If the manufacturer/organization wishes detailed documentation to be in the Public Domain, a note will be added to the Registry, but they will be responsible for such publication.

**E7 Ownership**

The DMX512 Standards are copyrighted. By registering a START Code or Manufacturer ID, no ownership rights are conferred to any third party. Alternate START Codes are registered to particular entities solely to allow for orderly management of the Standard. The registrant does not own the Alternate START Code or Manufacturer ID.

*-end of Annex E-*

*- end of Standard -*